

General Description

SDC4569A is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in sub 60W range.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. Under no load or light load condition, the IC operates in extended burst mode to minimize switching loss, Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with SDC4569A. A large value resistor could thus be used in the startup circuit to minimize the standby power.

The internal slope compensation improves system large signal stability and reduces the possible subharmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense(CS) input removes the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design.

SDC4569A offers complete protection coverage with automatic self-recovery feature including cycle-by-cycle current limiting (OCP), over load protection (OLP), VDD over voltage clamp and under voltage lockout (UVLO). The gate drive output is clamped to maximum 12V to protect the power MOSFET.

Features

- Frequency shuffling technology for improved EMC performance
- Audio noise free operation
- Extended burst mode control for improved efficiency and minimum standby power design
- External programmable pwm switching
- Internal synchronized slope compensation
- Low VDD startup current and low operating current
- Leading edge blanking on current sense input
- Good protection coverage with auto self-recovery (UVLO/OVP/OCP/OLP)
- Package: SOP-8

Applications

- Battery charger
- Power adaptor
- Set-top box power supplies

Pin Configuration

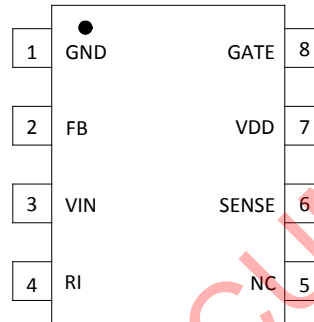
SOP-8


Figure 1. Pin Configuration

| Pin No. | Pin Name | Function |
|---------|----------|--|
| 1 | GND | Ground |
| 2 | FB | Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input |
| 3 | VIN | Connected through a large value resistor to rectified line input for startup IC supply |
| 4 | RI | Internal Oscillator frequency setting pin. A resistor connected between RI and GND set the PWM frequency |
| 5 | NC | - |
| 6 | SENSE | Current sense input pin. Connected to MOSFET current sensing resistor node |
| 7 | VDD | Chip DC power supply pin |
| 8 | GATE | Totem-pole gate drive output for the power MOSFET |

Table 1. Pin Description

Functional Block Diagram

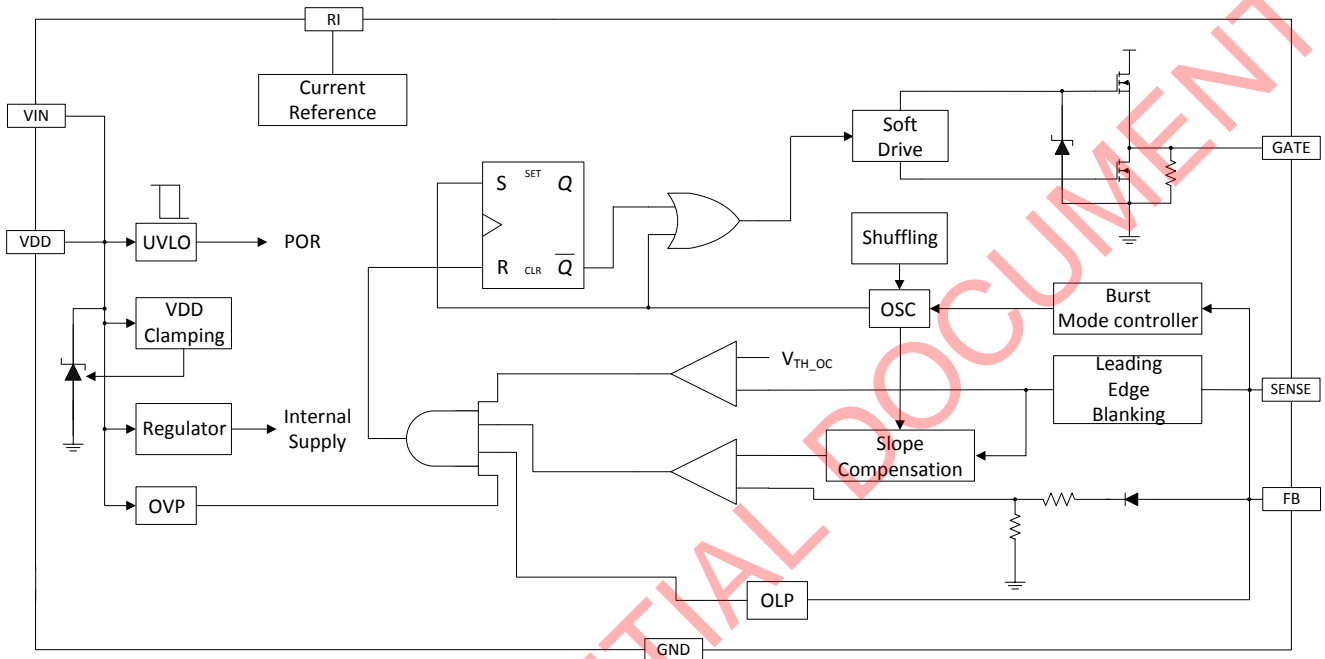
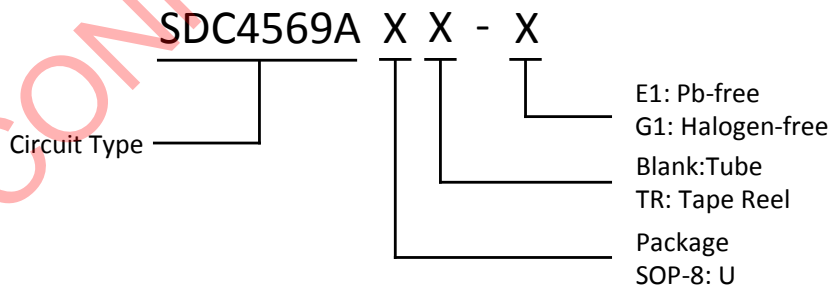


Figure 2. Functional Block Diagram

Ordering Information



| Package | Part Number | | Marking ID | | Packing Type |
|---------|----------------|----------------|------------|--------------|--------------|
| | Pb-free | Halogen-free | Pb-free | Halogen-free | |
| SOP-8 | SDC4569AUTR-E1 | SDC4569AUTR-G1 | 4569A | 4569AG | Tape Reel |

Absolute Maximum Ratings (NOTE: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device.)

| Parameter | Symbol | Value | Unit |
|--|-----------------|---------|------|
| VDD DC supply voltage | V_{DD} | -0.3~30 | V |
| VDD clamp voltage | V_{DD_CLAMP} | 32 | V |
| VDD DC clamp current | I_{CLAMP} | 10 | mA |
| V_{FB} input voltage | V_{FB} | -0.3~7 | V |
| SENSE input voltage | V_{SENSE} | -0.3~7 | V |
| V_{RI} input voltage | V_{RI} | -0.3~7 | V |
| Operating junction temperature T_J | T_J | 150 | °C |
| Storage temperature T_{STG} | T_{STG} | -55~150 | °C |
| Latch-up test per JEDEC 78 | - | 200 | mA |
| ESD,HBM model per Mil-Std-883H,Method 3015 | HBM | 2000 | V |
| ESD,MM model per JEDEC EIA/JESD22-A115 | MM | 200 | V |

Table 2. Absolute Maximum Ratings

Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|-----------------------------|-----------|-----|-----|------|
| VDD DC supply voltage | V_{DD} | 10 | 30 | V |
| Oscillation frequency | f_{OSC} | 60 | 70 | kHz |
| Operating Temperature Range | T_{OP} | -40 | 85 | °C |

Table 3. Recommended Operating Conditions

Electrical Characteristics ($T_a=25^\circ\text{C}$, unless otherwise specified)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|-----------------|---|-----|-----|-----|------|
| Supply Voltage (VDD) | | | | | | |
| VDD start up current | $I_{STARTUP}$ | $V_{DD}=12.5\text{V}$, $RI=24\text{k}$ Measure Leakage current into VDD | - | 3 | 20 | uA |
| Operation current | I_{DD} | $V_{DD}=16\text{V}$, $RI=24\text{k}$, $V_{FB}=3\text{V}$ | - | 1.4 | - | mA |
| VDD under voltage lockout enter | $V_{UVLO(ON)}$ | - | 6.5 | 7.5 | 8.5 | V |
| VDD under voltage lockout exit (recovery) | $V_{UVLO(OFF)}$ | - | 13 | 14 | 15 | V |
| VDD zener clamp voltage | V_{DD_CLAMP} | $I_{DD}=10\text{mA}$ | 30 | 32 | 34 | V |

Electrical Characteristics (Ta=25°C, unless otherwise specified)(Continued)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|-------------------|---|------|------|------|------|
| Feedback Input Section(FB pin) | | | | | | |
| FB open loop voltage | V_{FB_OPEN} | - | - | 4.8 | - | V |
| FB pin short circuit current | I_{FB_SHORT} | Short FB pin to GND and Measure Current | - | 0.8 | - | mA |
| Zero duty cycle FB threshold voltage zero | V_{TH_OD} | $V_{DD}=16V, RI=24k$ | - | - | 0.85 | V |
| Power limiting FB threshold voltage | V_{TH_PL} | - | - | 3.7 | - | V |
| Power limiting debounce time | t_{D_PL} | - | - | 35 | - | ms |
| Maximum duty cycle | DC_{MAX} | $V_{DD}=16V, RI=24k, FB=3V, CS=0$ | 70 | 80 | 90 | % |
| Current Sense Input(Sense Pin) | | | | | | |
| Leading edge blanking time | $t_{BLANKING}$ | $RI = 24K$ | - | 300 | - | ns |
| Over current detection and control delay | t_{D_OC} | $V_{DD} = 16V, CS > V_{TH_OC}, FB=3.3V$ | - | 75 | - | ns |
| Over current threshold voltage at zero duty cycle | V_{TH_OC} | $FB=3.3V, RI=24k$ | 0.70 | 0.75 | 0.80 | V |
| Oscillator | | | | | | |
| Normal oscillation frequency | f_{OSC} | $RI=24k$ | 60 | 65 | 70 | kHz |
| Frequency temperature stability | Δf_{TEMP} | $V_{DD}=16V, RI=24k, Ta=-20^{\circ}C \sim 100^{\circ}C$ | - | 5 | - | % |
| Frequency voltage stability | Δf_{VDD} | $V_{DD}=12V \sim 25V, RI=24k$ | - | 5 | - | % |
| RI open load voltage | V_{RI_OPEN} | - | - | 2 | - | V |
| Burst mode base frequency | f_{BM} | $V_{DD} = 16V, RI = 24k$ | - | 22 | - | kHz |
| Soft start time | t_{SOFT} | - | - | 7 | - | ms |
| Gate Drive Output | | | | | | |
| Output low level | V_{OL} | $V_{DD}=16V, I_o=-20mA$ | - | - | 0.8 | V |
| Output high level | V_{OH} | $V_{DD}=16V, I_o=20mA$ | 10 | - | - | V |
| Output clamp voltage level | V_{CLAMP} | - | - | 12 | - | V |
| Output rising time | t_r | $V_{DD}=16V, CL=1nf$ | - | 125 | - | ns |
| Output falling time | t_f | $V_{DD}=16V, CL=1nf$ | - | 50 | - | ns |
| Frequency Shuffling | | | | | | |
| Shuffling frequency | f_{OSC} | $RI=24k$ | - | 64 | - | Hz |
| Modulation range/Base frequency | Δf_{OSC} | $RI=24k$ | -3 | - | 3 | % |

Table 4. Electrical Characteristics

Function Description

The SDC4569A is a highly integrated PWM controller IC optimized for offline flyback converter applications in sub 65W power range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of SDC4569A is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet provides reliable startup in application.

Operating Current

The operating current of SDC4569A is low at 1.4mA. Good efficiency is achieved with SDC4569A low operating current together with extended burst mode control features.

Frequency shuffling for EMI improvement

The frequency shuffling/jittering (switching frequency modulation) is implemented in SDC4569A. The oscillation frequency is modulated with a random source so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore reduces system design challenge.

Extended Burst Mode Operation

Under zero load or light load condition, meet of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time, Reducing switching frequent leads to the reduction on power loss and thus conserves the energy.

SDC4569A self adjusts the switching mode according to

the loading condition. Under no load to light/medium load condition, the FB input drops below burst mode threshold level, device enters burst mode control. The gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state, otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in kΩ range at nominal loading operational condition.

$$f_{osc} = \frac{1560}{RI(k\Omega)} (kHz)$$

Current Sensing and Leading Edge Blanking

Cycle-by-cycle current limiting is offered in SDC4569A current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation.

This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

SDC4569A Gate is connected to an external MOSFET gate for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time

control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 12V clamp is added for MOSFET gate protection at higher than expected VDD input.

Protection Controls

Good power supply system reliability is achieved with its rich protection features including cycle-by-cycle current limiting (OCP), over load protection (OLP) and over voltage clamp, under voltage lockout on VDD (UVLO).

Typical Application

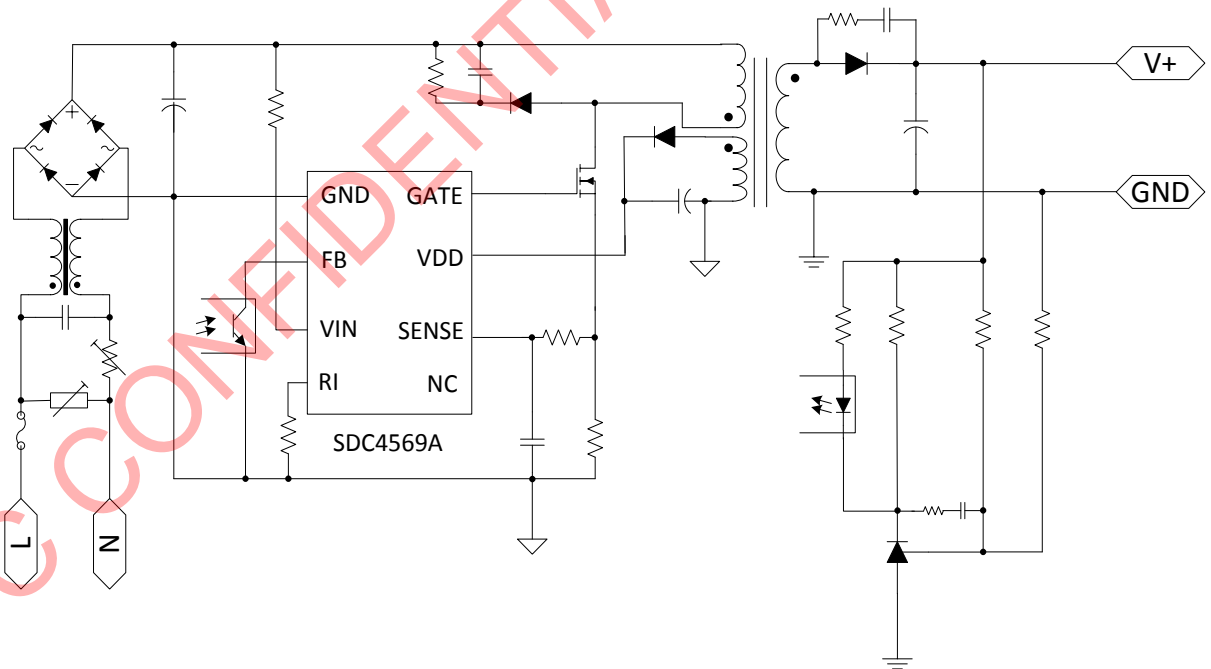
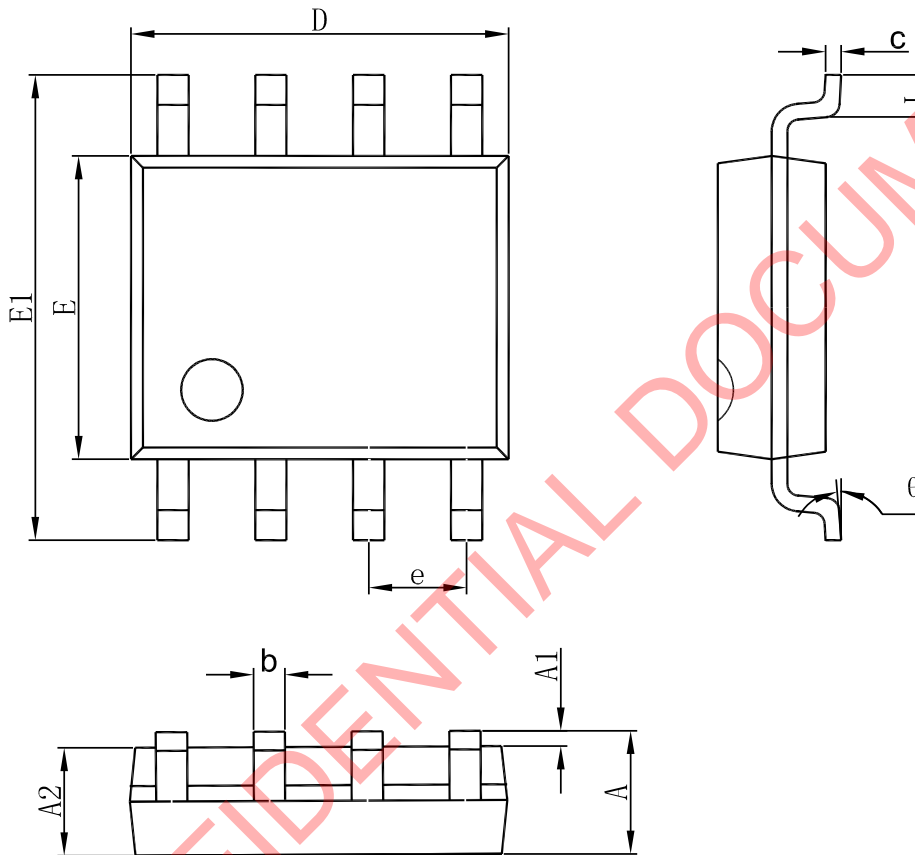


Figure 3. Typical Application

Package Dimension
SOP-8


| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.201 |
| e | 1.270(BSC) | | 0.050(BSC) | |
| E | 5.800 | 6.200 | 0.228 | 0.244 |
| E1 | 3.800 | 4.000 | 0.150 | 0.157 |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |



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<http://www.sdc-semi.com/>

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